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Design of a low-power flash analog-to-digital converter chip for temperature sensors in 0.18 μm CMOS process

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ABSTRACT. Current paper proposes a simple design of a 6-bit flash analog-to-digital converter (ADC) by process in 0.18 µm CMOS. ADC is expected to be used within a temperature sensor which provides analog data output having a range of 360 mV to 560 mV. The complete system consisting of three main blocks, which are the threshold inverter quantization (TIQ)-comparator, the encoder and the parallel input serial output (PISO) register. The TIQ-comparator functions as quantization of the analog data to the thermometer code. The encoder converts this thermometer code to 6-bit binary code and the PISO register transforms the parallel data into a data series. The design aims to get a flash ADC on low power dissipation, small size and compatible with the temperature sensors. The method is proposed to set each of the transistor channel length to find out the threshold voltage difference of the inverter on the TIQ comparator. A portion design encoder and PISO registers circuit selected a simple circuit with the best performance from previous studies and adjusted to this system. The design has an input range of 285 to 600 mV and 6-bit resolution output. The chip area of the designed ADC is 844.48 x 764.77 μm^2 and the power dissipation is 0.162 μW with 1.6 V supply voltage.

Keywords: flash ADC, temperature sensors, serial output.

Projeto de um conversor analógico-digital flash de baixa potência para sensores de temperatura em processo CMOS a 0,18 μm

RESUMO: Este trabalho propõe um projeto simples de um conversor analógico-digital (ADC) flash de 6-bits por processo de CMOS a 0,18 µm. Este dispositivo está previsto para ser usado dentro de um sensor de temperatura, o que proporciona uma saída analógica de dados dentro de intervalo de 360 mV a 560 mV. O sistema completo consiste em três blocos principais, que são o comparador de tipo (TIQ)-quantização de inversor de limiar, o codificador e o registrador de saída serial, a parte de entrada em paralelo (PISO). O comparador (TIQ) funciona como quantização dos dados analógicos para termômetro. O codificador converte este código de termômetro para código binário de 6-bits e o registrador PISO transforma os dados paralelos em uma série de dados. O objetivo do projeto é obter um ADC flash com baixa dissipação de potência, tamanho pequeno e compatível com os sensores de temperatura. O método é proposto para definir o comprimento de cada canal de transistor, para encontrar a diferença de tensão de limiar do inversor em cada comparador TIQ. Foram selecionadas partes de um codificador circuito registrador PISO em um circuito simples, e apresentaram melhor desempenho em relação aos estudos anteriores e foram ajustados a este sistema. O projeto tem um intervalo de entrada de 285-600 mV e saída de resolução de 6-bits. A área do chip do ADC projetado é 844,48 x 764,77 μm^2 e a dissipação de energia é 0,162 µW, com tensão de alimentação de 1,6 V.

Palavras-chave: ADC flash, sensores de temperatura, saída serial.

Introduction

Technological developments and use of wireless-system applications with low power consumption have become one of the main attractions in circuit design. Explosive growth of embedded sensor into radio frequency identification (RFID) tag is nowadays used with low voltage supply. Sensor data, integrated into the RFID systems, require ADC circuits. The ADC design presented in this paper is a converter suitable for a temperature sensor. The temperature sensor is implanted on the RFID-Tag chip, which is integrated into the RFID or wireless system. The design is expected to have lower power dissipation and operating voltage, small area size and easy to integrate with the other circuits. The ADC which is in accordance with that purpose is a Flash-ADC by TIQ-Comparator application. The Flash-ADC has many advantages, such as high speed, high linearity, low voltage and reduced power dissipation (YOO et al., 2003). Previous researches have undertaken a variety of methods to get the best performance of ADC, as Table 1 shows.

Table 1 shows that previous research generally developed design flash ADC with the lowest power

Table 1. Comparison of results of ADCs design.

References	Design				
	Architecture / Method	CMOS Technology (μm)	Supply Voltage (V)	Power dissipation (μW)	Layout Area (μm^2)
(YOO et al., 2003)	Flash / TIQ technique	0.25	2.375 to 2.65	35250	228
(DALY; CHANDRAKASAN, 2009)	Flash / comparator redundancy	0.18	0.2 to 0.9	1.66	1960000
(WU et al., 2012)	SAR / Res-Cap	0.13	1.2	1200	100000
(SAHOO; RAZAVI, 2009)	Pipeline / precision resistor	0,09	1.2	348000	1360000
(KULKARNI et al., 2010)	Flash / extend the TIQ	0.18	1.8	36980	-
(SHAHRAMIAN et al., 2009)	Flash / data trees	0.35	5	500000	-
(AGRAWAL; PAILY, 2010)	Flash / TIQ technique	0.18	1.8	20000	8000000
(RAJPUT; KANATHE, 2012)	Flash / TIQ technique and sh circuit	0.35	2.5	5000	-
(SENTHIL; BANUPRIYA, 2012)	Flash / sh circuit	0.18	1.8	5300	-
(CHUN et al., 2009)	Flash / reference voltage and common mode calibration	0.065	1.2	4000	130000
(YOUNG et al., 2012)	Flash / Time domain comparator	0.18	1.8	8000	132000

dissipation of 1.66 µW proposed by (DALY; CHANDRAKASAN, 2009). Further, (WU et al., 2012) proposed the SAR ADC design method with a power dissipation of 1200 µW and (SAHOO; RAZAVI, 2009) proposed a method pipeline ADC with 348 mW power dissipation, but they did not get a lower power consumption compared to the flash ADC. Current research proposed a low power dissipation flash ADC design with TIQ-comparator, encoder and PISO register development to obtain the best performance which is compatible for use with the temperature sensor system.

Material and methods

The complete system of flash ADC consists of three main blocks, or rather, TIQ comparator, encoder and PISO registers, as shown in Figure 1.

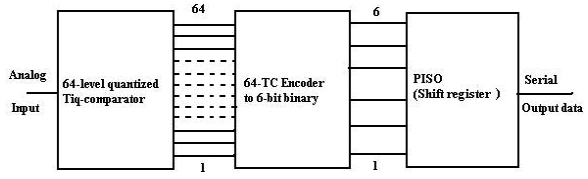

Figure 1. Block diagram of the flash ADC.

The TIQ-Comparator is functioning as data quantization of the analog data to thermometer code (TC), and is important for linearity and accuracy of the data transfer. The encoder makes sharper thresholding of comparator output and provides full digital output voltage swing and converting to 6-bit binary code. The PISO register works to process 6-bit of parallel to serial data.

The temperature sensor will use this design at a range between -100 and 200°C. The sensor has a range analog output from 285 to 560 mV with the supply voltage 1.6 V and 31.14 μW power consumption. This sensor was developed on our previous research and match to input of flash ADC propose.

A basic TIQ Comparator circuit consists of two cascaded CMOS inverters, as shown Figure 2 (YOO et al., 2003). The first inverter works as voltage reference to the ADC system. The second inverter works as the gain booster to keep linearity in balance from the voltage rising and falling intervals (YOO et al., 2003).

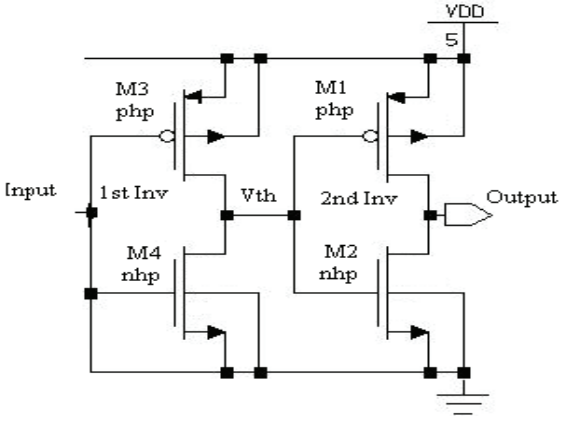

Figure 2. Basic TIQ-Comparator.

In previous researches several methods for design of TIQ-comparator have been studied, such as: the analog input signal quantization level is set in the first stage by changing the voltage transfer curve (VTC) by transistor sizing (TANGEL; CHOY, 2004) and (SUDAKAR et al., 2011), the size of both transistor channel lengths, L and width, W are adjusted (YOO et al., 2003), third, by only adjusting W and L is fixed (TANGEL; CHOY, 2004).

Current research applies to another method by adjusting L and keeping W fixed. The advantages of this method are reduced power consumption and area of the layout. Increasing L reduces the transistor drain current, I_D according to (UYEMURA, 1988**)** for a transistor in saturated condition as:

$$I_D = \frac{1}{2}\frac{\mu_n \varepsilon_{ox}}{t_{0x}}\frac{W}{L}[2(V_{GS} - V_{tn})V_{DS} - V_{DS}^2] \quad (1)$$

where:

I_D is transistor drain current;
μ_n is electron mobility;
εox is permittivity of the silicon dioxide;
$t ox$ is the transistor channel width layer;
W is transistor channel width;
L is transistor channel length;
V_{GS} is voltage gate–source,
V_{tn} is voltage threshold,
V_{DS} is voltage drain-source.

The main design of TIQ comparator is to convert analog data to 64-level thermometer data code as a block diagram in Figure 3. This design is referred to that to obtain n-bit flash ADC is 2^n-1 comparator (KHOT et al., 2012). Therefore it is necessary to design a 6-bit Flash ADC as much as (2^6)-1 = 63 TIQ comparators. Meanwhile, to get the CMOS transistor channel 'L' of each first inverter refers to the mathematical expression of the threshold voltage (V_{th}) of any quantized sub-unit can be derived approximately as equation (2) (RAJASHEKAR; BHAT, 2009).

$$V_{th} = \frac{V_{DD} - |V_{tp}| + V_{tn}\sqrt{\frac{K_n}{K_p}}}{1 + \sqrt{\frac{K_n}{K_p}}} \quad (2)$$

In this case, V_{tn} and V_{tp} are the threshold voltages for NMOS and PMOS devices respectively. In this equation, $K_n = (W L^{-1})_n \mu_n C_{ox}$ and $K_p = (W L^{-1})_p \mu_p C_{ox}$. The μ_n and μ_p are the whole and electron mobility of NMOS and PMOS respectively.

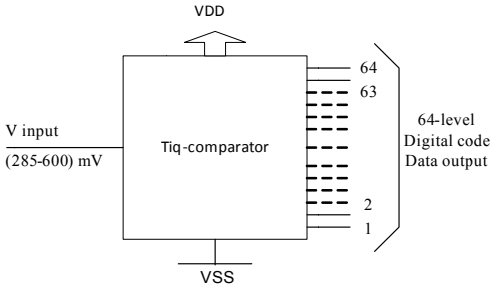

Figure 3. Block diagram of the TIQ-comparator.

Development of the comparator was based on the basic circuit given in Figure 2 and equation (2). Equation (2) was used to calculate 'L' of the PMOS transistor channel of the first inverter according to the desired value of the threshold voltage. The result is shown in Table 2. In the calculation, the range of the threshold voltage should be compatible with the output voltage of the sensor within the range 360 - 560 mV.

Further implementation of the design is done as follows: PMOS transistor's W on the first inverter is made on 1.4 μm fixed, whereas the channel length is different and these techniques are followed to the next inverters, according to Figure 4. However, NMOS of all inverters' remain at the same ratio of W and channel L. The calculation is made starting from most significant bit (MSB) of quantized to the least significant bit (LSB) with the value of Vth, 600 to 285 mV.

Table 2. Calculation result of the PMOS transistor channel length and width of the first inverter .

Size	The number of the TIQ-comparator																				
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
Channel length, L (μm)	0.51	0.54	0.58	0.62	0.66	0.71	0.78	0.84	0.92	1.08	1.11	1.2	1.32	1.45	1.60	1.75	1.95	2.16	2.38	2.62	2.91
Channel width, W (μm)	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4	1.4

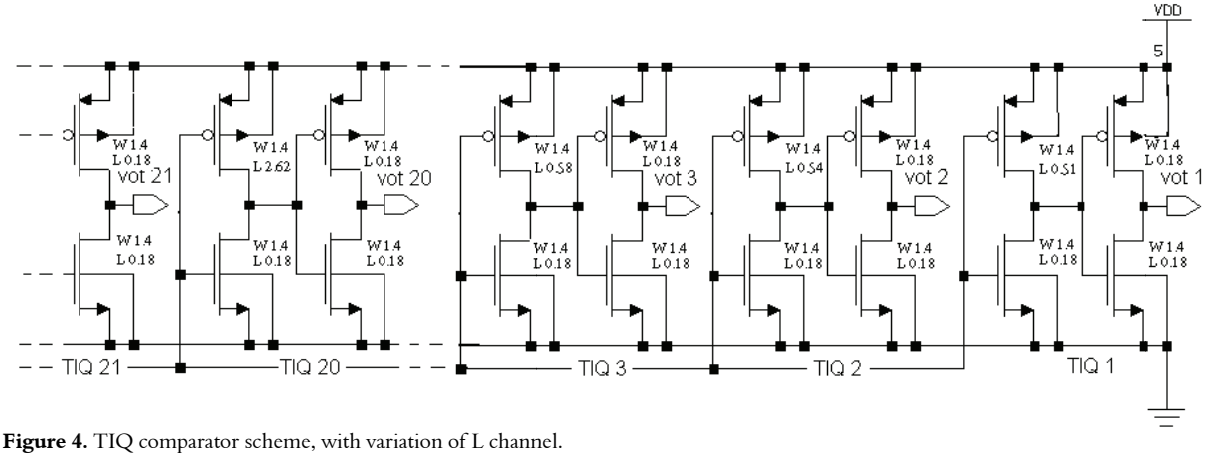

Figure 4. TIQ comparator scheme, with variation of L channel.

In this calculation, the size of the channel L for the TIQ-comparator No. 1 to 21 only is obtained, with channel L from 0.51 μm to 2.91 μm, as shown in Figure 4.

For the next comparator No. 22 to 64 one or two PMOS transistors are inserted as compensation in diode connection to complement the achievement of the expected voltage input range to the lower side. The compensation transistor is inserted between VDD to the first inverter PMOS transistors, as shown in Figure 5. Meanwhile, the design size of the L and channel W of the second inverter are fixed, according to the design standard of the 0.18 - μm CMOS Technology. The standard design is 0.18 μm of L and 1.4 μm of W for PMOS and NMOS transistors respectively.

In previous researches, there are many methods for the design of the encoder circuit. There are; Fat-tree encoder (RAJESWARI et al., 2012); MUX-based encoder (ARUNKUMAR et al., 2012) and (SANDNER et al., 2005); bubble error correction (BEC) circuit; ROM-based encoder (KULKARNI et al., 2010); logic-based encoder (KUMAR; KOLHE, 2011). All the methods propose the same advantages such as high speed, high resolution, low power and etc. Logic-based encoder is the best performance and matches the proposed design. Due in this design, there are two main points that are low power and simple circuit. For the benefits of low power and simple circuit, the encoder is implementing the circuits by using CMOS logic gates in CEDEC standard library. In this process, the encoder has two functions that are used to eliminate the bubble-error and convert 64-level thermometer code into 6-bit binary code. The bubble error is the result of many sources, for instance, clock jitter, device mismatch, offset voltage. The input thermometer code of a circuit is invalid code and there is no correction circuit; consequently output of the ADC in this case is incorrect.

Circuits of the encoder proposal consist of gray code circuits and decoder circuits. The gray circuit contains NOT, AND and OR gate configuration, as Figure 6 shows.

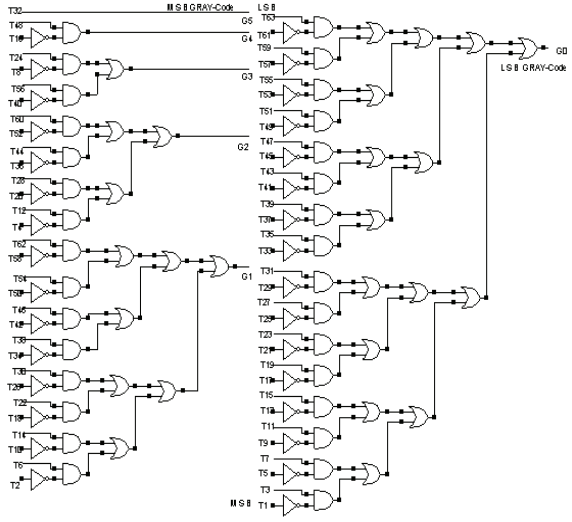

Figure 6. Gray Code Circuits.

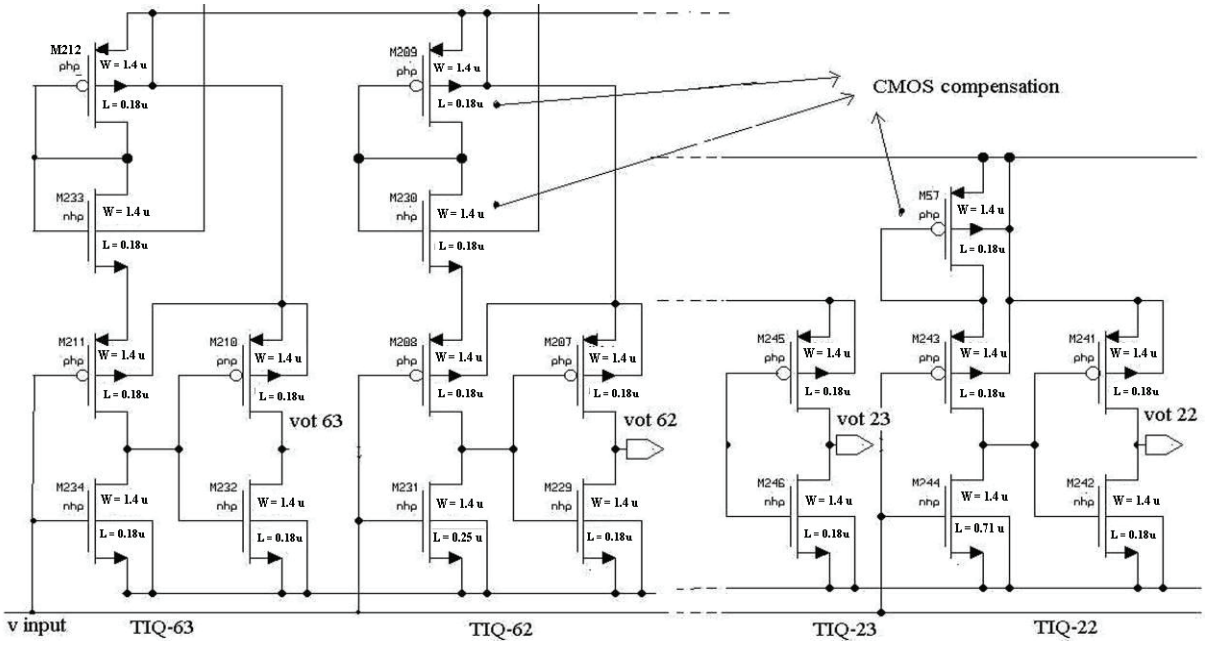

Figure 5. TIQ Comparator with CMOS compensation.

The decoder circuits contain EXOR-gate configuration, as Figure 7 shows.

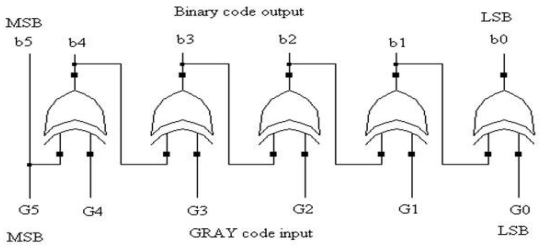

Figure 7. Decoder Circuits

The conversion of 64-level TC into BCs is shown in Table 3. Boolean´s algebra may be expressed as:

G5 = T32, G4 = T48.T16, G3 = T56.T40 + T24.T8 , G2 = T60.T52 + T44.T36 + T28.T20 + T12.T4 , G1 = T62.T58 + T54.T50 + T46.T42 + T38.T34 + T30.T26 + T22.T18 + T14.T10 +T6.T2 , G0 = T63.T61 + T59.T57 + T55.T53 + T51.T49 + T47.T45 + T43.T41 + T39.T37 + T35.T33 + T31.T29 + T27.T25 + T23.T21 + T19.T17 + T15.T13 + T11.T9 + T7.T5 + T3.T1 .

where,

T is a thermometer code in which T64 is LSB and T1 is MSB.

G is a gray code, in which G0 is LSB and G5 is MSB. In the following expressions b is the binary code where b0 is LSB and b5 is MSB.

b5 = G5 b4 = G5 (+) G4 b3 = b4 (+) G3 b2 = b3 (+) G2
b1 = b2 (+) G1 b0 = b1 (+) G0

Table 3. Thermometer code to gray code and to 6-bit code.

	Thermometer Code								Gray Code					6-bit binary					
No.	T64	T63	T62	-	T32	-	T4	T3	T2	T1	G5	G4	G3	G2	G1	G0	b0	b1	b2	b3	b4	b5
1	0	0	0	-	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	-	0	-	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1
3	0	0	0	-	0	-	0	0	1	1	0	0	0	0	1	1	0	0	0	0	1	0
4	0	0	0	-	0	-	0	1	1	1	0	0	0	0	1	0	0	0	0	0	1	1
5	0	0	0	-	0	-	1	1	1	1	0	0	0	1	1	0	0	0	0	1	0	0
-	-	-	-	-	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
32	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0
-	-	-	-	-	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
62	0	0	1	-	1	-	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0	1
63	0	1	1	-	1	-	1	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0
64	1	1	1	-	1	-	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1

Parallel input serial output (PISO) register functions as converting parallel 6-bit binary to serial output as Table 4 demonstrates. The low power of shift register design was proposed by (ANDRAWES et al., 2009), where they used D flip-flop in weak inversion region. D flip-flop was used for the efficient design of the register. In this design, the PISO register circuit was configured from D-FF with load and clock control, as Figure 8 indicates. The two controls arrange data shifting into the shift-register system.

Table 4. Parallel 6-bit binary to serial on 1 byte data.

CLK	Parallel Data Input						Serial Output
	B5 (MSB)	B4	B3	B2	B1	B0 (LSB)	
0	1	0	1	0	1	0	X
1	X	1	0	1	0	1	0 LSB
2	X	X	1	0	1	0	1
3	X	X	X	1	0	1	0
4	X	X	X	X	1	0	1
5	X	X	X	X	X	1	0
6	X	x	X	X	X	X	1 MSB

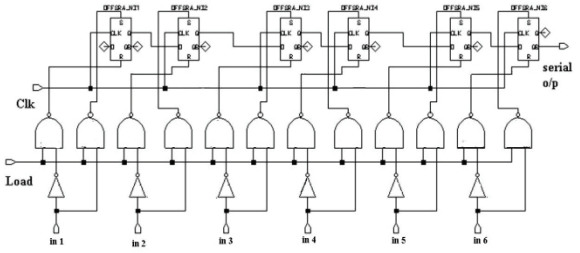

Figure 8. 6-bit PISO Register.

Results and Discussion

The circuit design is designed and simulated by using the tools of the Mentor Graphics Design Architect (DA) CEDEC_KIT. The design and simulations are carried out to achieve repeatedly a linear quantization value. To obtain a linear quantization value in the simulation of 0.0 V to 0.61 V, it is given by the DC input signal, as in Figure 9, while to obtain a frequency response of quantization from 1 to 10 KHz, it is given by the AC signal input, shown by Figure 10.

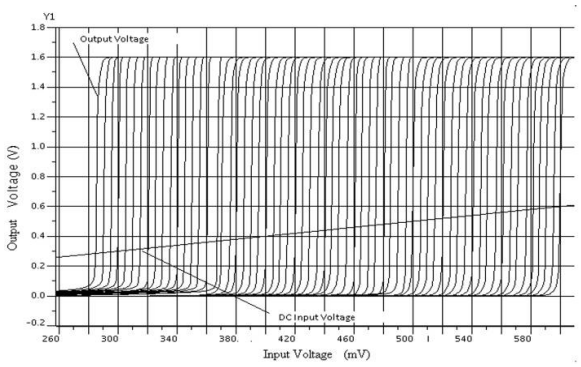

Figure 9. Output quantization between 0.0 and 0.6 V DC input range

Figure 9 shows the conversion of analog input to quantization output responding range between 0.285 V and 0. 6 V. During the increment of 5 mV in the DC input, the quantization output increases 1 level. These phenomena are convincing to quantify the analog data temperature sensor with range between 0.36 and 0.56V only.

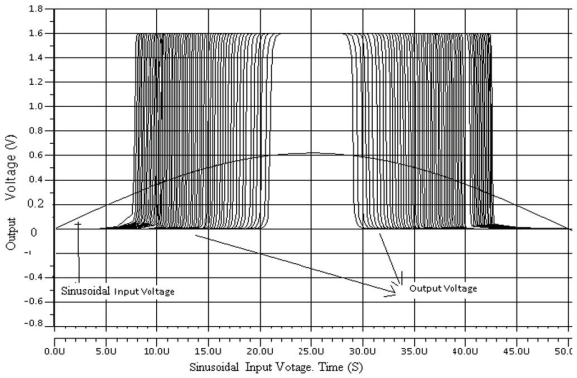

Figure 10. Output quantization of the AC input 10 KHz.

Figure 10 illustrates the simulated quantization result of the TIQ Comparator designed with the sinusoidal input voltage between 0V and 0.6 V-peak at the frequency 10 KHz and half wave positive transition. This graphical response exhibits a good linearity and sensitivity with linear rise and fall of the input signal.

The Encoder output graph is shown in Figure 11. This output is result simulation synchrony to Figure 8 and match to Table 3 of design principle.

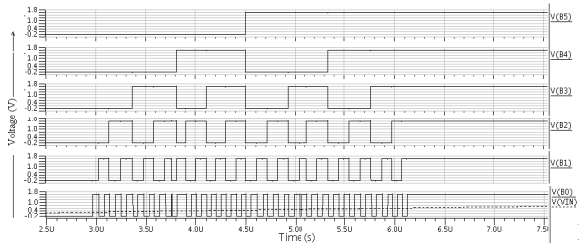

Figure 11. The encoder output graph with the signal input rising.

Figure 12 shows simulation results of PISO registers with 6 bit binary parallel input and serial output. Pulse clock (V clock) functions as a shift control on register and pulse load (V load) for reset of the register every one byte data transfer.

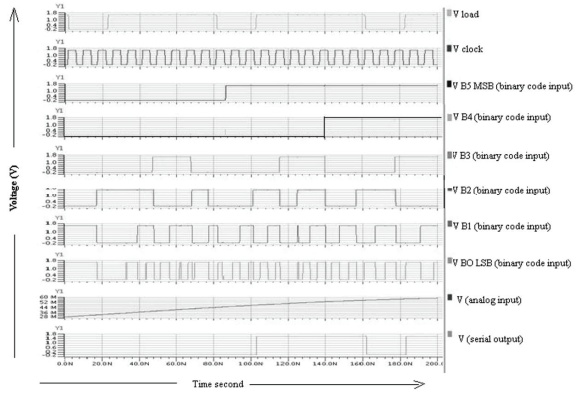

Figure 12. The simulation results of PISO registers.

Figure 13 shows simulation results of complete flash ADC with 0 to 0.6 V analog input, 100 MHz clock pulse and 10 MHz Load pulse. Simulation results show that the planning works properly so that it may change the analog data to serial linearly.

Based on Figure 13, status DC characteristic integral non linear (INL) and differential non linear (DNL) may be calculated, as shown in Figure. 14. The results show that the maximum INL is 3 mV or 0.6 LSB and maximum DNL is 2 mV or 0.4 LSB.

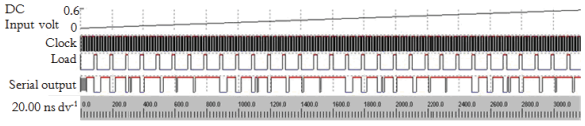

Figure 13. The simulation result of complete flash ADC.

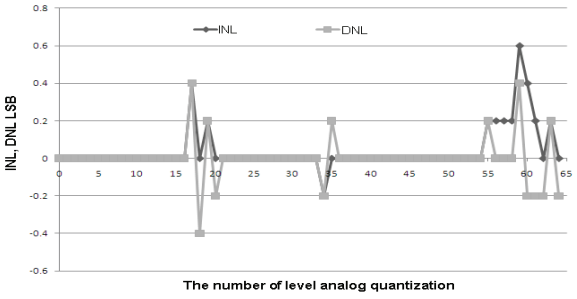

Figure 14. The deviation of analog quantization to serial output.

The final layout design chip is shown in Figure 15. This chip consists of three main blocks, or rather, TIQ-comparator, encoder and PISO register. Around the circuit is added pad terminal to connect the circuits with the power supply as well as input and output pin. All of the blocks of the flash ADC integrated in this chip, with the layout size 844.48 x 764.77 μm^2.

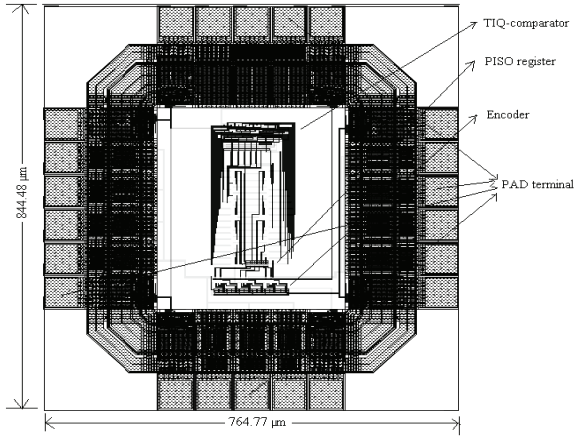

Figure 15. The final layout design chip.

Table 5 shows the comparative results of proposed ADC with the other flash ADC architectures. It may be noted that the proposed design has the lowest power dissipation which emphasizes an innovative challenge. The layout area design was shown in Figure 14 with the pad terminal included, whereas the other designs are featured by excluding pad terminal. However, this layout size of the pad depends on the library CEDEC standard design. Hence, the proposed design did not appear in the smallest layout size in Table 5.

Table 5. Comparison of the propose design with other flash ADCs.

References	Design				
	Architecture / Method	CMOS Technology (μm)	Supply Voltage (V)	Power dissipation (μW)	Layout Area (μm^2)
(YOO et al., 2003)	Flash / TIQ technique	0.25	2.375 to 2.65	35,250	228
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(KULKARNI et al., 2010)	Flash / extend the TIQ	0.18	1.8	36,980	-
(SHAHRAMIAN et al., 2009)	Flash / data trees	0.35	5	500,000	-
(AGRAWAL; PAILY, 2010)	Flash / TIQ technique	0.18	1.8	20,000	8,000,000
(RAJPUT; KANATHE, 2012)	Flash / TIQ technique and sh circuit	0.35	2.5	5000	-
(SENTHIL; BANUPRIYA, 2012)	Flash / sh circuit	0.18	1.8	5300	-
(CHUN et al., 2009)	Flash / reference voltage and common mode calibration	0.065	1.2	4,000	130,000
(YOUNG et al., 2012)	Flash / Time domain comparator	0.18	1.8	8,000	13,2000
Proposed design	Flash / TIQ Comparator	0.18	1.6	0.162	645,832

Conclusion

The flash ADC is designed and verified by using the Mentor Graphics VLSI Design Software. The final chip is designed by CEDEC Industry Standard I/O Cell Library for Fabrication Lab Silterra Malaysia. It consists of 64 pairs of CMOS inverters in the-TIQ comparator part, the logic based is used for the encoder part, and D-type flip-flop for the PISO register develop. The design has an input range of 285 to 600 mV and 6-bit resolution output. The chip area of the designed ADC is 844.48 x 764.77 μm^2. The power dissipation is 0.162 μW in 1.6 V supply voltage and the sinusoidal input voltage of 0V to 0.6 V-peak at the 10 KHz frequency and positive half wave transition condition. The design is suitable for use to the wireless temperature sensor system.

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