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A 0.13 µm CMOS V-band Cascode Low Noise Amplifier with Custom Transmission Line Inductors

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ABSTRACT. This paper presents the design of a 60 GHz low noise amplifier (LNA) compliant with the IEEE 802.11ay network standards. The proposed LNA employs SilTerra 0.13 µm RF CMOS technology (April 2018 version) for its design and is developed based on the single-stage cascode topology. The performance of the design has been optimized using the source degeneration technique with gain-boosting and middle inductors. Due to the limitations of the process design kit (PDK), custom inductors have been developed for the LNA circuit. The inductors use ultra-thick metal (UTM) with a copper thickness of 3.3 µm. At 60 GHz, the proposed LNA has a simulated input reflection coefficient (S_{11}) of -15.71 dB, reverse gain (S_{12}) of -15.83 dB, forward gain (S_{21}) of 7.25 dB, output reflection coefficient (S_{22}) of -8.78 dB, noise figure (*NF*) of 6.79 dB and minimum noise figure (NF_{min}) of 6.55 dB. It is also unconditionally stable at 60 GHz with a simulated Rollett stability factor (*K*) of 1.27 and B1 stability factor of 0.79. The design shows high linearity, with a simulated input 1-dB compression point ($P1dB$) of -12.31 dBm and third order input intercept point ($IIP3$) of -3.09 dBm. The LNA has a 3-dB bandwidth of 9.3304 GHz, spanning from 55.35 GHz to 64.68 GHz. The power dissipation (*PD*) and supply voltage (V_{DD}) of the LNA are 7.34 mW and 1.2 V, respectively.

Keywords: V-band, LNA; transmission lines; RF CMOS; millimetre wave; 5G.

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Introduction

In radio frequency (RF) receivers, low noise amplifiers (LNAs) are used to amplify the magnitude of the incoming signal received by the antenna. As can be seen in the literature, deep submicron metal oxide semiconductor field effect transistors (MOSFETs) with sizes ranging from 0.18 µm to 22 nm have been widely implemented in the development of LNA circuits (Liu et al., 2024; Khyalia et al., 2024; Kim & Kwon, 2012; Balasubramaniam et al., 2024; Lin et al., 2014; Wang et al., 2015; Lin & Lee, 2015; Priyanka et al., 2021; As & Yelten, 2023; Lin et al., 2023; Das & Ramanaiah, 2024). Owing to its high speed and gate density as well as wide accessibility, SilTerra's 0.13 µm Radio Frequency Complementary Metal Oxide Semiconductor (CL130MR), embedded within the 0.13 µm CMOS Logic Generic (CL130G) process design kit (PDK), is among the popular technologies adopted for this purpose (Leong et al., 2020; Eshghabadi et al., 2016).

As wireless communication technologies march inexorably towards their fifth generation (5G), the CL130G PDK proves inadequate in fully supporting designs operating at frequencies higher than 30 GHz. For ultra-high-speed mobile broadband, the 5G technologies operate from approximately 6 to 100 GHz (Mishra, 2018). Having operating frequencies about 100-fold higher than its 4G counterpart, the components required for their LNA circuits are comparatively more demanding than those used in the 4G LTE networks. Although endeavours have been made to develop millimetre wave LNAs using Silterra's PDK, all of which (to the best of the authors' knowledge) fail to produce convincingly good results.

Studies on the CL130G PDK have revealed that the primary drawback that hampers its implementation in the 5G technology is the limited geometry options and electrical performance of its reactive components – particularly the inductors. While the scalable inductors provided by the PDK are relatively comprehensive for circuits operating in the microwave regime, they are uncharacterized beyond 30 GHz. Besides, the inductor geometries found in the PDK are only restricted to the rectangular and octagonal spiral shapes. Although Yao et al. (2007) show that spiral inductors produce good Q-factors in the millimetre wave, the width used in the design is as small as 2 µm. Such width is simply too narrow to be fabircated using the CL130G PDK (the minimum width of the ultra-thick metal or UTM layer specified in the PDK is 2.5 µm).

This paper presents the design of a 60 GHz LNA using the CL130G PDK. The unlicensed 60 GHz band is supported by the IEEE 802.11ay standard and is therefore instrumental in realizing the 5G wireless network (Nguyen et al., 2019; Aggarwal et al., 2021). In order to allow the circuits to be designed using SilTerra's PDK, five custom inductors that operate below 130 pH at 60 GHz are developed. As will be demonstrated in the subsequent sections, the LNA produces good results in the millimetre wave band.

Material and methods

Owing to its efficacy in suppressing issues ensuing from the Miller effect, the cascode topology has been a popular option for LNAs operating at higher frequencies. In comparison with the conventional common-gate (CG) and common-source (CS) topologies, the cascode topology also produces relatively lower noise figure (*NF*), higher linearity, broader bandwidth, higher stability (i.e., K > 1), better isolation (i.e. higher S_{12} value), higher gain (i.e. higher S_{21} parameters), as well as better immunity to variations in the external environment.

Figure 1 shows the schematic of the proposed LNA circuit. As can be seen from the figure, an inductance L_M sandwiched between the two NMOS transistors is introduced. The introduction of the L_M inductor provides several advantages for the design – it helps to eliminate the middle pole of the cascode configuration, compensate the relatively low transit frequency (f_t) of the transistors (Yao et al., 2007) and improve the S_{22} parameter. The parameters of the components are tabulated in Table 1.

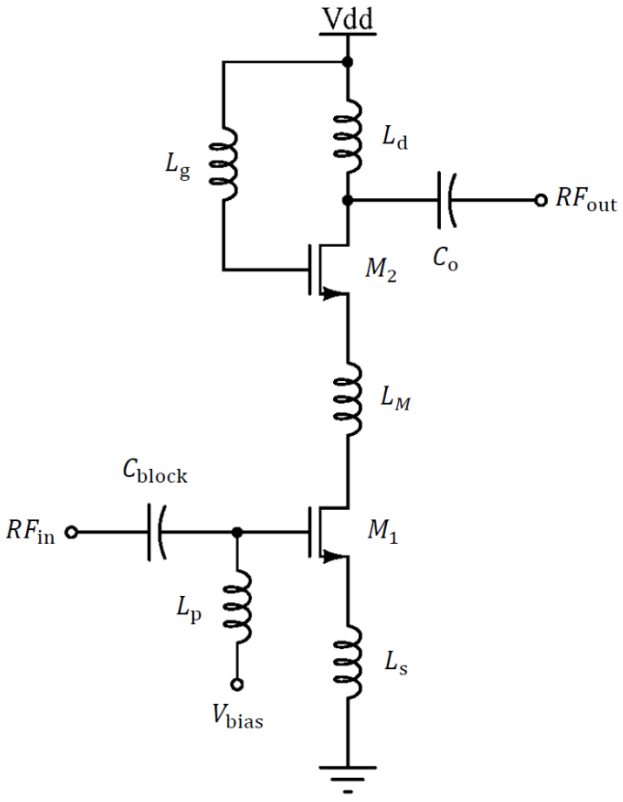

Figure 1. Schematic of the proposed LNA.

Table 1. Components of the LNA in Figure 1.

Components	Values
M_1 and M_2	L= 0.13 µm, finger = 27, finger width = 1.5 µm, total width = 40.5 µm
C_o	25 fF
C_{block}	200 fF
L_s	60 pH
L_g	65 pH
L_p	90 pH
L_d	100.2083 pH
L_M	125.6pH

The design of the proposed LNA circuit has been modified from the source degeneration cascode topology in Leong et al. (2020). Two n-type MOSFET (NMOS) transistors have been connected in a cascade to realise the topology. To improve impedance matching at the input port, an inductor (L_S) is connected to the source of the input transistor. The width, length, and the number of fingers are already determined from Hassan et al. (2014). Wideband matching at the millimetre waves is made possible by manipulating the gate-drain capacitance (C_{gd}), which depends on the transistor model. Figure 2 shows the simplified transistor model of the input transistor in the proposed LNA. By solving the circuit using Kirchhoff's current law (KCL) (Wang et al., 2015), the input admittance (Y_{in}) of the circuit can be expressed as

$$Y_{in} = \left(\frac{g_m L_S}{C_{gs}} + sL_s + \frac{1}{sC_{gs}}\right)^{-1} + \left(Z_M + \frac{1}{sC_{gd}}\right)^{-1} + \left(sL_s + \frac{s^2 C_{gs} L_S}{g_m} + \frac{1}{g_m} + \frac{L_S}{C_{gd} Z_M} + \frac{sC_{gs}L_S}{C_{gd} g_m Z_M} + \frac{1}{sC_{gd} g_m Z_M}\right)^{-1} \quad (1)$$

where $s = j\omega$ is the complex frequency, ω the angular frequency, g_m the transconductance of the transistor, L_S the source degeneration inductor, C_{gd} the gate-drain capacitance, C_{gs} the gate-to-source capacitance and Z_M is the equivalent output impedance of the input transistor. Upon simplification, Y_{in} in (1) can be presented in terms of the sum of the following three impedances:

$$Z_1 = \frac{g_m L_S}{C_{gs}} + sL_s + \frac{1}{sC_{gs}}, \quad 2)$$

$$Z_2 = Z_M + \frac{1}{sC_{gd}}, \quad (3)$$

$$Z_3 = sL_s + \frac{s^2 C_{gs} L_S}{g_m} + \frac{1}{g_m} + \frac{L_S}{C_{gd} Z_M} + \frac{sC_{gs}L_S}{C_{gd} g_m Z_M} + \frac{1}{sC_{gd} g_m Z_M}, \quad (4)$$

where

$$Z_M = \left(g_{m_2} + g_{mb_2}\right)^{-1} + \frac{Z_L}{(g_{m_2} + g_{mb_2}) R_{ds_2}}. \quad (5)$$

In (5), R_{ds_2} denotes the resistance between the drain and the source of M_2.

It can also be seen from Figure 3 that, the resistance R_M, inductance L_M and capacitance C_M are in parallel, i.e.

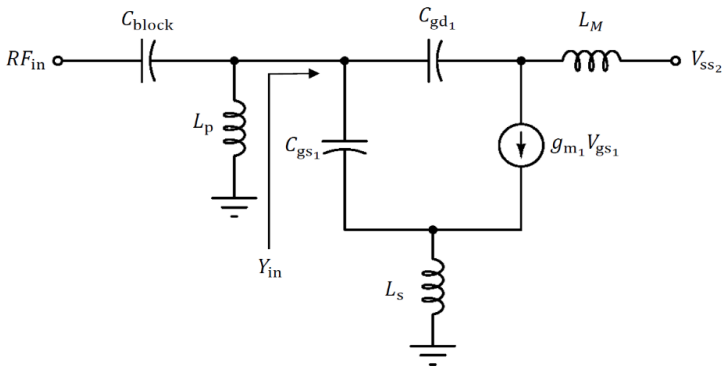

Figure 2. Small-signal equivalent circuit of the input transistor.

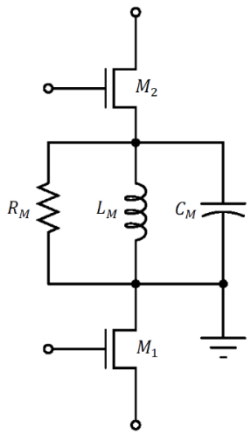

Figure 3. Lumped circuit of the middle inductor L_M.

$$Z_L = R_M \parallel sL_M \parallel \frac{1}{sC_M} \quad .(6)$$

By solving (2) to (4), the resonance frequencies f_1, f_2, and f_3 can be obtained as

$$f_1 = \frac{1}{2\pi\sqrt{(L_g+L_s)C_{gs}}}, \quad (7)$$

$$f_2 = \frac{1}{2\pi\sqrt{L_g C_{gd}}}, \quad (8)$$

$$f_3 = \frac{1}{2\pi\sqrt{\left[L_g+\left(1+\frac{C_{gs}}{C_{gd}g_m Z_M}\right)L_s\right]C_{gd}g_m Z_M}}. \quad (9)$$

In (7), the conventional matching point emerges due to the presence of L_S. The resonance frequency in (9) is much higher than that of the operational band and therefore R_2 can be omitted. For f_3, the real part of Z_3 is denoted as

$$Re\{Z_3\} = \frac{1}{g_m} + \frac{L_s}{C_{gd}Z_M}. \quad (10)$$

In general, g_m^{-1} approaches 50 Ω which is similar to the case of the common-gate input matching scenarios. Therefore, the second term in (10) should be as small as possible. Given that the first term of equation (2) results in 50 Ω, $g_m Z_m$ satisfies the condition in (11),

$$g_{\mathrm{m}} Z_M \gg \frac{C_{\mathrm{gs}}}{C_{\mathrm{gd}}} \quad (11)$$

This shows that if Z_M is sufficiently high, a second input matching point will be introduced at f_3, which is far lower than f_1. This allows a wideband input matching characteristic to be formed in the circuit. By virtue of this, L_M is able to widen the bandwidth of the LNA. Besides, the Miller effect introduced by C_{gd} will have a more significant impact if the gain of the LNA increases. Therefore, a Z_M with large value is needed to provide a high voltage gain from the drain to the gate. This can be achieved by introducing passive loads to the CS transistor, such as connecting an *LC* network or T-shaped networks to the gate of the transistor.

Selecting the appropriate inductance value for L_M in Figures 1 to 4 is important since it provides wideband matching for the circuit and also stabilizes the circuit. This is possible because the inductor tunes out the parasitic capacitances (Pan et al., 2019) such as the source capacitance of M_2 (C_{S2}) and the drain capacitance of M_1 (C_{d1}) as shown in Figure 4. Without L_M, both capacitances would not be shorted and the wire between both NMOS transistors would have a low output impedance. This causes RF current to flow through the low impedance wire and directly to the ground, essentially shorting M_1. By adding L_M, the capacitance effects are neutralised (Wang et al., 2015).

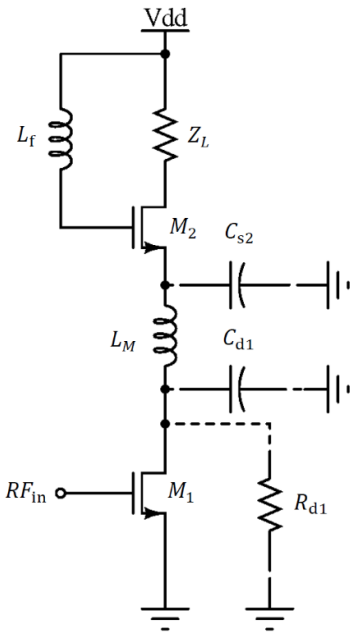

Figure 4. Illustration for the tuning of middle inductor (L_M) and the gate feedback inductor (L_f).

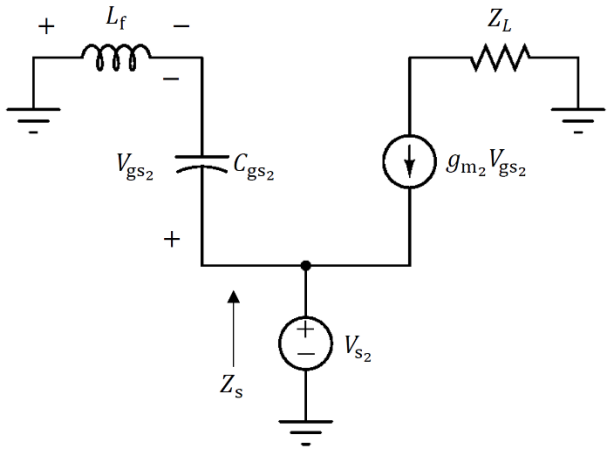

Figure 5. Small-signal equivalent circuit of M_2.

The gate inductor at M_1 (L_g) serves as the gain boosting inductor for the LNA circuit. It introduces positive feedback to C_{gs2} and increases the voltage across it, as shown in Figure 5. Hence, L_g is denoted as a feedback inductor (L_f) in this section. The voltage across L_f is the inverse of V_{gs} and the relationship between V_{gs} and V_s is

$$V_{gs} = \frac{V_s}{1-\omega^2 L_f C_{gs_2}}. \tag{12}$$

The input impedance Z_S at the gate of M_2 is shown in (13) below (Wang et al., 2015)

$$Z_s = \frac{1-\omega^2 L_f C_{gs_2}}{g_{m_2}+j\omega C_{gs_2}}. \tag{13}$$

Upon inspecting (13), it can be seen that Z_S decreases as ω increases. More current from the drain of M_1 will then flow to the source of M_2, which in turn, enhances the transconductance of the cascode amplifier ($g_{cascode}$). It can also be seen from Figure 4 that, the output resistance at the drain of the input transistor (R_{d1}) also drains part of the current to ground. Since L_M has already tuned out both C_{d1} and C_{S2}, then g_{cascode} can be mathematically expressed as (Wang et al., 2015)

$$g_{cascode} = \frac{I_{out}}{V_{in}} = \frac{(g_{m_2}+j\omega C_{gs_2})g_{m_1}R_{d_1}}{(1-\omega^2 L_f C_{gs_2})+(g_{m_2}+j\omega C_{gs_2})R_{d_1}}. \tag{14}$$

It is apparent from (14) that, $g_{cascode}$ approaches the value of g_{m1} when frequency f is sufficiently high. Since the cascode amplifier has a larger output resistance compared with other single-ended amplifiers, such as the common source topology, a higher gain can be achieved with this technique. Despite having these benefits, however, the inductance of L_f should be carefully selected (i.e. not too large) as this topology is known to have potential instability introduced by negative resistance when $\omega > \omega_r$ (Wang et al., 2015). In (15), the resonance frequency ω_r is defined as

$$\omega_r = \left(\sqrt{L_f C_{gs_2}}\right)^{-1}. \tag{15}$$

Since CL130G (PDK version April 2018) fails to synthesise inductors below 110 pH to operate at 60 GHz (Leong et al., 2020), the five inductors depicted in Table 1 had to be designed separately and subsequently incorporated into the proposed LNA design. One of the most popular methods in designing inductors operating in the millimetre wave band is by using transmission lines (Božanić & Sinha, 2018). Due to its simplicity and high Q-factor at millimetre wave frequencies, a ribbon inductor has been employed here. To reduce skin effect and to maintain a relatively compact geometry design, the width (w) of each custom ribbon inductor was set to 10 µm. The length (l) of the ribbon inductor can be estimated by numerically solving for the root of the transcendental equation in (16) below (Golio, 2000)

$$\mathrm{L} = 0.125\mathrm{l}\left[\ln\left(\frac{2\mathrm{l}}{\mathrm{w}}\right) + 0.5 + \frac{2\mathrm{w}}{9\mathrm{l}}\right] \times 10^{-6}. \tag{16}$$

It is to be noted that (16) is derived with the thickness of the substrate assumed to be infinite. In reality, metallisation is performed at the ultra-thick metal (UTM) layer and the physical substrate thickness of this process is 700 µm. Hence, the results obtained from (16) could only be used as an approximation for the design. Subsequent parametric adjustments are to be performed using an electromagnetic solver such as the Sonnet Suites™, in order to obtain the targeted inductance values. Tables 2 and 3 show the length and Q-factor of

the custom ribbon inductors and their corresponding inductance values at 60 GHz. It is to be noted that, the inductances have been tailored to be somewhat lower than their targeted values in Table 1. The purpose of doing so is to account for the coupling of parasitic inductances induced by the presence of interconnects and vias. Figure 6 shows the performance of the ribbon inductors within ±10 GHz from its operating 60 GHz. It is apparent from the figure that, the inductances show good selectivity (i.e., the Q-factors are above 45) at the extremely high frequency (EHF) range and are literally invariant of frequency.

Table 2. Targeted inductances and lengths of the inductors in Figure 1.

Inductor	Targeted Inductance at 60 GHz (pH)	Length (μm)
L_s	60	99.4
L_g	65	105.6
L_p	90	133.2
L_d	100.2083	143.79
L_M	125.6	167.5

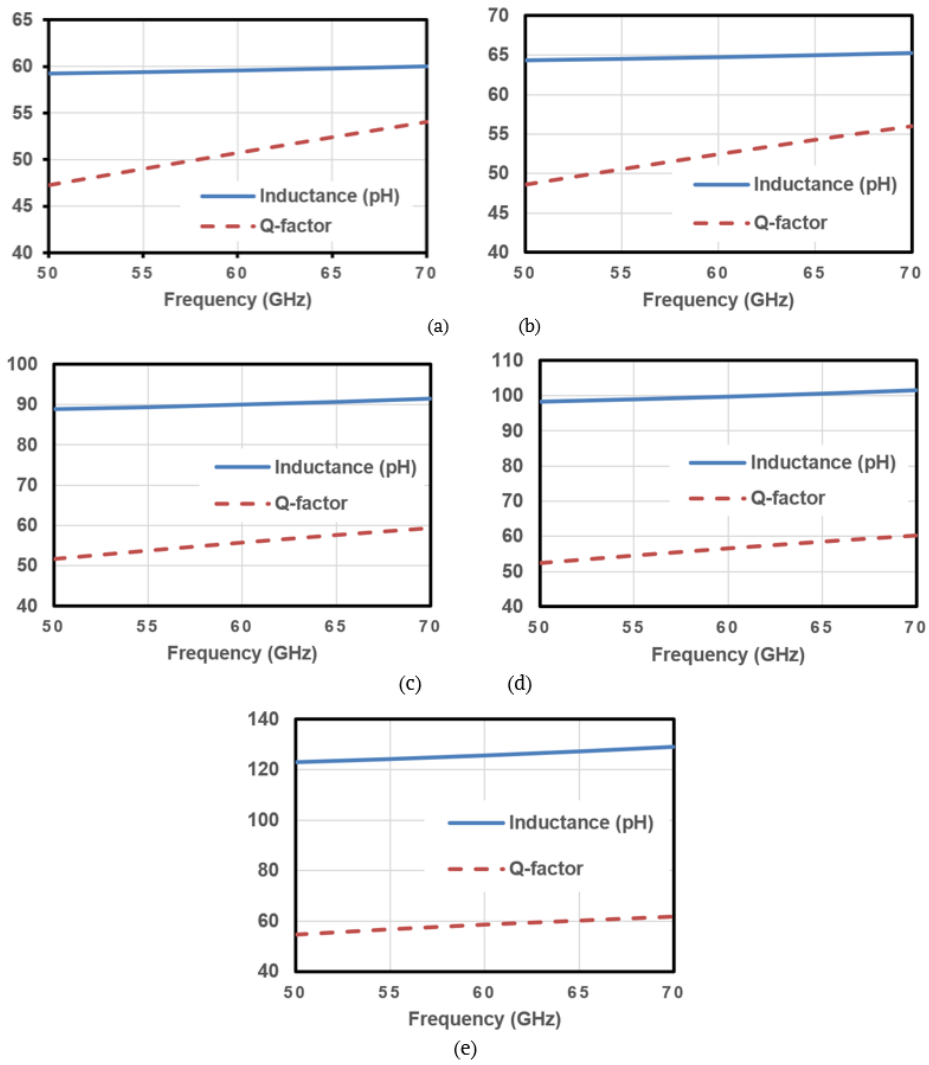

Figure 6. Simulated inductances and Q-factors of (a) L_s, (b) L_g, (c) L_p, (d) L_d, and (e) L_M.

Table 3. Simulated inductances and Q-factors of the inductors in Figure 1.

Inductor	Simulated Inductance at 60 GHz (pH)	Simulated Q-factor at 60 GHz
L_s	59.57	50.73
L_g	64.74	52.44
L_p	89.99	55.71
L_d	99.7	56.53
L_M	125.6	58.57

Results and discussion

In order to validate the performance of the proposed LNA design, the custom ribbon inductors were integrated with the LNA circuit and simulated using Cadence Virtuoso. The proposed LNA has a power dissipation of 7.34 mW and it draws 6.11 mA from a 1.2 V source. The simulated S-parameters are shown in Figure 7. Upon close inspection of the S_{11} input reflection coefficient, it can be seen that the LNA circuit shows good impedance matching – particularly at frequencies beyond 52.45 GHz, where S_{11} decreases below -10 dB. The S_{11} parameter drops to its minimum of -41.74 dB at 57.55 GHz and at 60 GHz, S_{11} = -15.71 dB. Likewise, the output reflection coefficient (S_{22}) curve shows a minimum of -8.84 dB at 59.75 GHz and at 60 GHz, S_{22} = -8.78 dB.

The S_{21} forward gain curve in Figure 7 shows that the LNA produces good frequency response, with its maximum of 7.264 dB at 59.7 GHz and 7.248 dB at 60 GHz. The 3-dB bandwidth of the proposed LNA is 9.33 GHz, which spans from approximately 55.35 to 64.68 GHz. Clearly, the bandwidth is large enough to accommodate ultra-wideband (UWB) technology. The circuit also shows excellent reverse isolation with its S_{12} reverse gain kept below -15 dB throughout the frequency range, with S_{12} = -15.83 dB at 60 GHz.

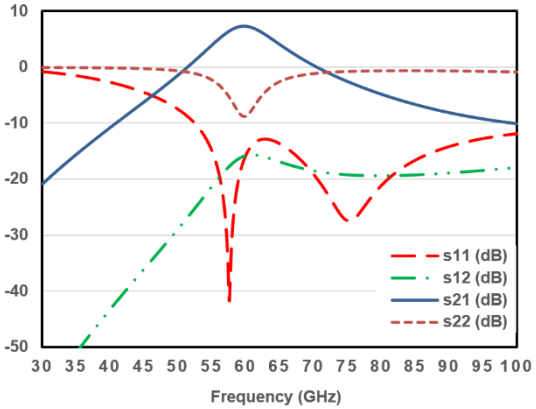

Figure 7. Simulated s-parameters of the proposed LNA.

Besides the scattering parameters, another important consideration in LNA designs is the various small-signal gains. Figure 8 depicts the operating power gain (G_P), transducer power gain (G_T) and available power gain (G_A) for the proposed LNA circuit. As can be seen from the figure, the gains of the proposed LNA are reasonably high. At 60 GHz, G_P, G_T and G_A are 7.366 dB, 7.248 dB and 7.866 dB respectively. It should be noted that, the result obtained for the transducer power gain is in agreement with that of the forward gain. It can also be observed from Figure 8 that the curves for both G_P and G_T match very well with each other. This further corroborates the fact that the impedance of the design is properly matched.

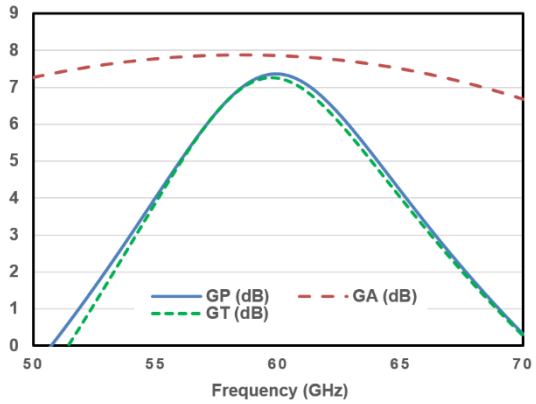

Figure 8. Simulated small-signal gains of the proposed LNA.

Noise figure (*NF*) is used to indicate the severity of noise interference. In order to ensure signal fidelity, the *NF* is to be maintained at a low level. Figure 9 depicts the *NF* and minimum *NF* (NF_{min}) of the circuit. At 60 GHz, the *NF* and NF_{min} are 6.79 dB and 6.55 dB, respectively. The parameters are comparable with those obtained from contemporary LNAs operating within the 50 to 70 GHz frequency range (Kim & Kwon, 2012; Wang et al., 2015; Lin & Lee, 2015; Huang, Lin, & Wang, 2009; Yeh et al., 2011).

As can be seen in Figure 10, the Rollett stability factor *K* and supplementary stability factor *B*1 exceed 1 and 0, respectively, when the LNA operates within the 3dB bandwidth. It can therefore be concluded that the LNA circuit is unconditionally stable at its operating range.

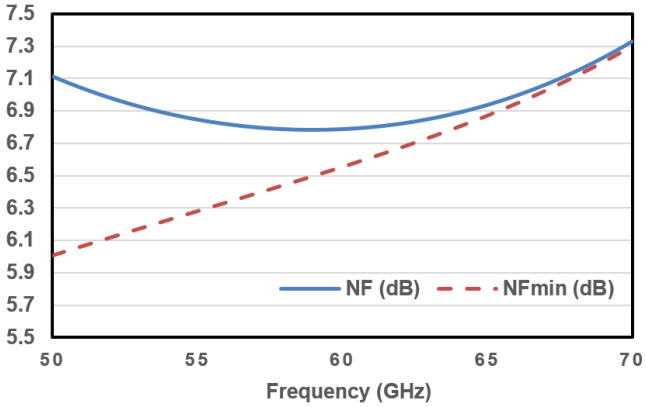

Figure 9. Simulated noise figures of the proposed LNA.

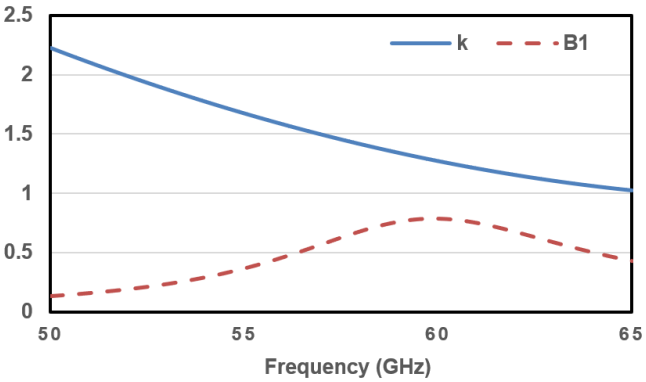

Figure 10. Simulated stability factors of the proposed LNA.

The 1-dB compression point (P1dB) curve is used to determine the compression point where the input power causes the gain to decrease 1 dB and deviates from the normal linear response. Figure 11 shows that with an input attenuation of -30 dBm and with a first order frequency of 60 GHz, the proposed LNA has an input P1dB of -12.3081 dBm. Clearly, the design has sufficiently high linearity and compression ratio to prevent distortion during its operation. A common approximation rule states that the third order input intercept point (IIP3) is approximately 10 dBm higher than that of the P1dB. For the proposed LNA, the two test tones are at 59.9 GHz and 60 GHz respectively. As shown in Figure 12, the IIP3 of the design lies at -3.08724 dBm. The difference between the simulated IIP3 and P1dB is 9.22086 dBm, which is acceptable for the 10-dB approximation rule.

Figure 13 illustrates the final layout of the LNA design. The entire layout (excluding bond pads) has a length of 471.5848 µm and a width of 239.4324 µm, which resulting in an active chip area of approximately 0.113 mm^2.

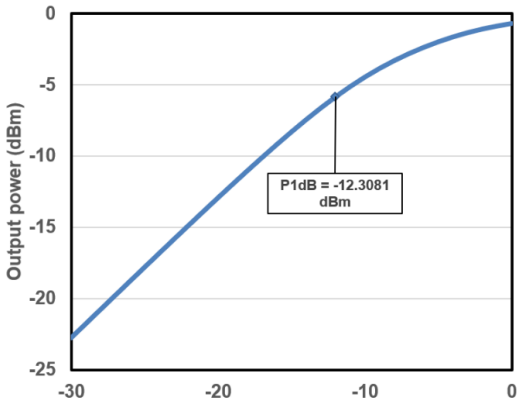

Figure 11. Simulated input 1-dB compression point (P1dB) of the proposed LNA.

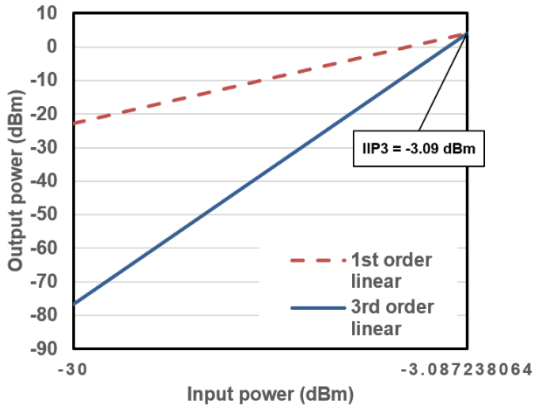

Figure 12. Simulated input third-order intercept point (IIP3) of the proposed LNA.

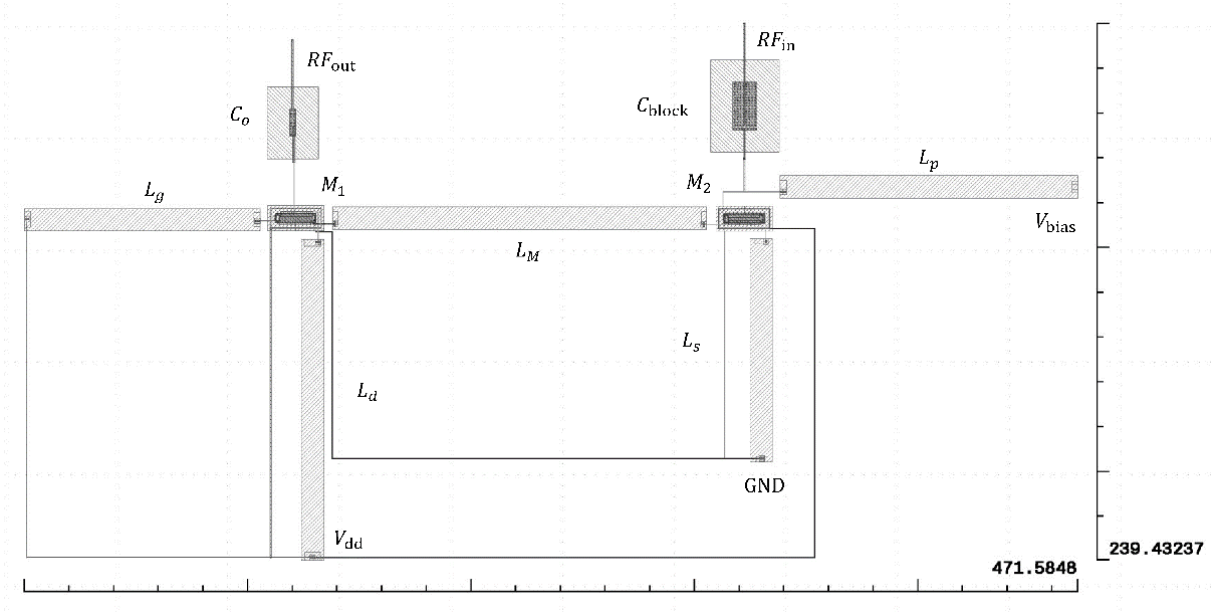

Figure 13. Layout of the proposed LNA excluding pads.

Conclusion

In this paper, the design of a LNA which operates at 60 GHz is presented. The design meets two of the criteria for the upcoming 802.11ay wireless standard: operating at 60 GHz and having a 3-dB bandwidth of more than 8.64 GHz (Ghasempouret al., 2017). The LNA circuit is based on the source degeneration cascode topology and employs 0.13 µm RFCMOS NMOS transistors. Five custom inductors below 130 pH have been developed and incorporated into the LNA circuit. The design has been validated using Cadence Virtuoso. The performance of the LNA is summarized in Table 4.

Table 4. Performance of the proposed LNA.

Parameter	Value
s_{11} (dB)	-15.71 at 60 GHz
s_{12} (dB)	-15.83 at 60 GHz
s_{21} (dB)	7.248 at 60 GHz
s_{22} (dB)	-8.77664 at 60 GHz
NF (dB)	6.7882 at 60 GHz
NF_{min} (dB)	6.5544 at 60 GHz
Stability	k = 1.27, $B1$ = 0.79, both at 60 GHz
P1dB (dBm)	-12.3
IIP3 (dBm)	-3.087
BW (GHz)	9.3304 (55.35 to 64.68)
PD (mW)	7.34ith V_{dd} = 1.2 V

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